library ieee;

use ieee.std\_logic\_1164.all;

use ieee.std\_logic\_unsigned.all;

use ieee.std\_logic\_arith.all;

entity comparator is

port(a,b: in std\_logic\_vector(1 downto 0);

Result: out std\_logic);

end comparator;

architecture comparator\_flux of comparator is

begin

process(a,b)

begin

if(a=b) then Result<='1';

else Result<='0';

end if;

end process;

end comparator\_flux;